Design Talk

Team: sddec23-08

Problem Statement

Ideal:

- Iowa State University would have access to fabricated ReRAM chips for research purposes
- Iowa State University would have institutional knowledge of how the analog design flow works for the Skywater 130nm process

Reality:

- It is difficult to get any fabricated chip, especially one with ReRAM, because of how new of a technology it is.
- Iowa State University has never produced a fabricated analog chip on the Skywater 130nm processed

Proposal:

- Use eFabless's MPW shuttle program to submit a ReRAM chip proposal.
    - If it gets approved, it would give us access to fabricated ReRAM chips
    - Along the way, we would document our workflow, contributing the ISU's internal knowledge of analog fabrication in the Skywater 130nm process.

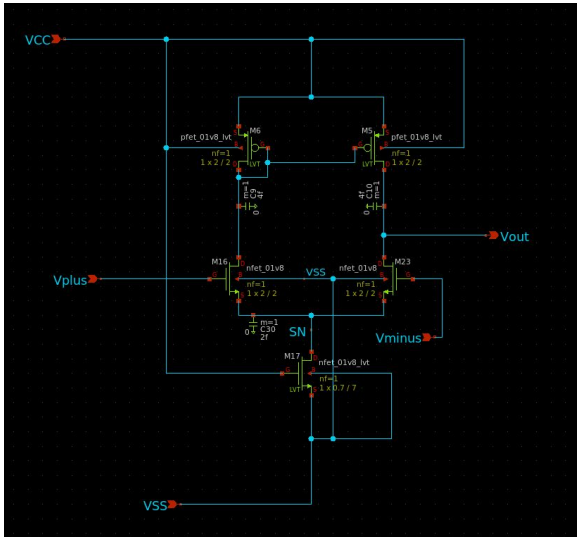
Design Context

- Client
  - Needs a ReRam crossbar for Testing and Research purposes
  - Wants Documentation on the Skywater 130nm process
- Students interested in ASIC chip design
  - Wants to learn more about bringing an integrated circuit through a design process to silicon
- Global, Cultural, Social and Economic
  - Open Source
- Environmental
  - ReRam is more power efficient than its digital counterparts

Design Context Continued…

Technical Complexity:

- ReRam cell
- Data Converters
- Op-Amps
- ASIC design
- Skywater 130nm Process flow



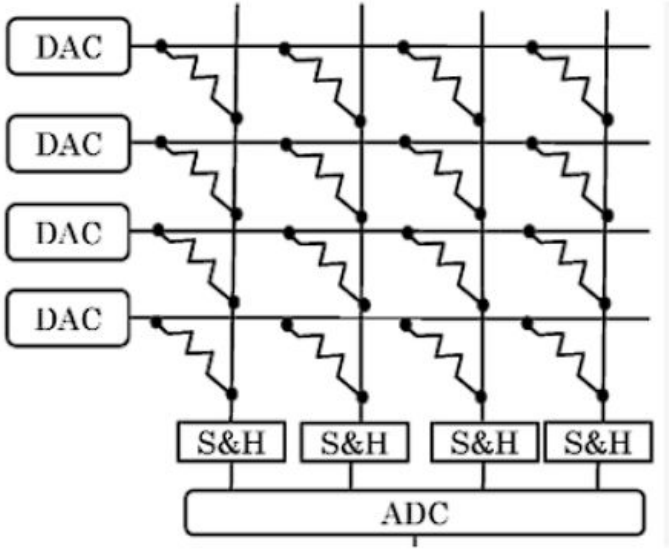
Design Exploration

- Key Decisions
  - Architecture of DAC
  - Architecture of ADC
  - How to write weights to 1t1R cells.
- Ideation of ADC architectures:
  - Successive Approximation ADC
  - Dual-Slope ADC
  - Pipeline ADC
  - **Flash ADC**
  - Delta-Sigma ADC

ADC Architecture	Pros	Cons
SAR	Handles waveshapes very well, takes very high sample rate, high resolutions	Can be slow, larger/more complex design at low resolutions
Dual-Slope	Very accurate, and has high-resolution	Slow sample rate and speed, can be hard to implement
Pipelined	Very fast speeds, good resolution	Inherent latency due to architecture
Flash	The fastest speed, no latency, easy to implement at "1-bit" level	Circuit gets much bigger with resolution increases, limited to 8-bit resolution
Delta-Sigma	Very high resolution, reduces quantization noise	Limited sample rate, does not handle unnatural waves

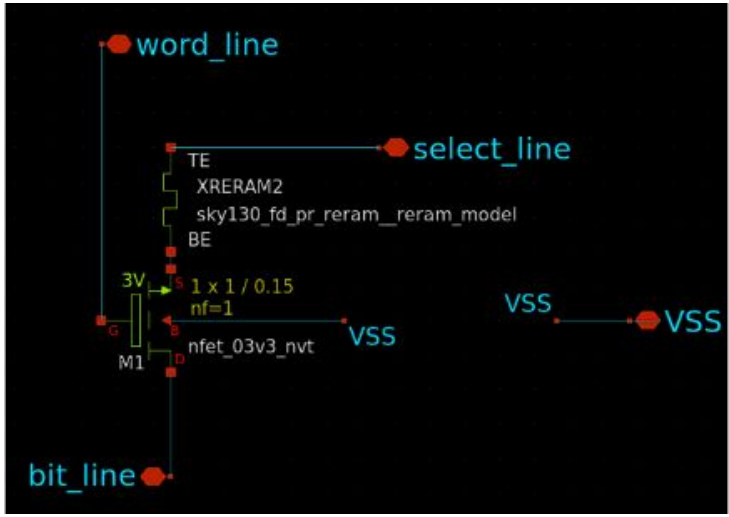
Proposed Design

- Timeline
  - User inputs digital value into circuit
  - Digital value gets turned into analog value through DAC
  - ReRAM crossbar does computation
  - Current accumulates on columns
  - Currents goes through transimpedance amplifier
  - Sample & Hold + ADC convert analog voltage back to digital value
  - Digital value is output to Caravel harness to be read by user



Proposed Design Continued…

- Each ReRAM cell is comprised of 1 ReRAM and 1 transistor (1t1R cell)
- Weights are written to gate of transistor (word_line)
  - This dictates if resistance is high or low for computation
- Select_line is the “rows”
  - This will be where output of DAC goes
- Bit_line is the “column”
  - Output of the cell where current accumulates



Design Analysis

- Currently in progress…
  - We have created DAC, ADC and 1t1R cell
  - Still need to create sample & hold circuit, and transimpedance amplifier
- For first test we are only running computation through one cell to ensure components work together as intended